Circuits in Emerging Nanotechnologies

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Chair: Adrian Ionescu, EPFL

Centre SI Integrated Systems Centre

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Symposium on Emerging Trends in Electronics

MONTREUX

DECEMBER 1-2 2014

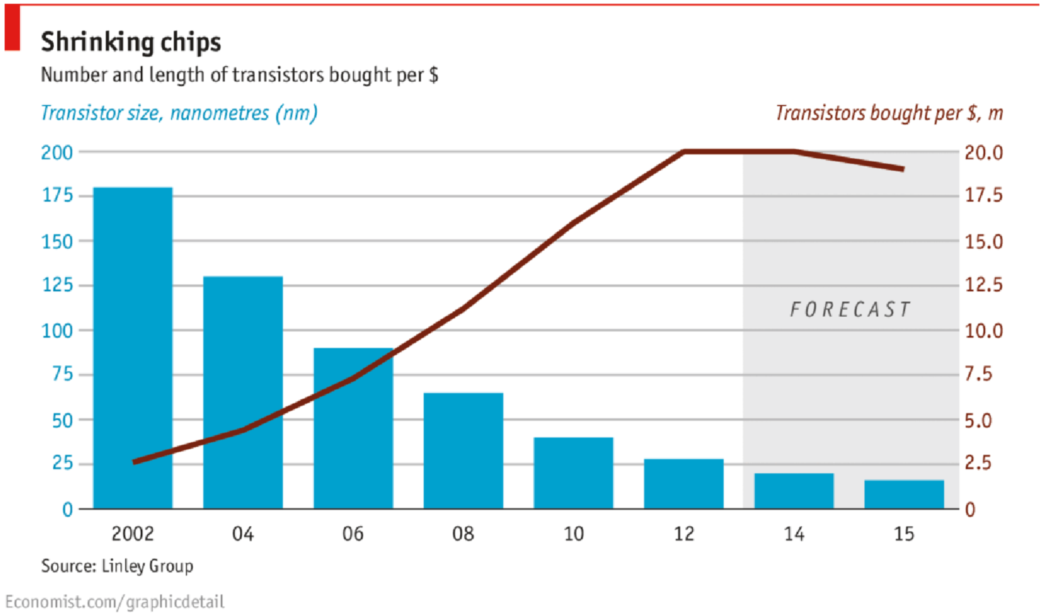
Panel on
Circuits in Emerging Nanotechnologies

Rinaldo Castello
University of Pavia Italy

EVOLUTION OF IC TECHNOLOGIES

Technology Aspects

Huge cost increase of advanced IC technologies.



Limited access to deeply scaled technologies for Research/Education

Competing technologies
FDSOI cheaper but can it scale?
FinFET can scale better

Result is slowing down of Moor's Law
Sweet spot technology Today 28nm LP Tomorrow 14 nm FDSOI?

OPPORTUNITIES OF TECHNOLOGY EVOLUTION
FOR ANALOG /RF DESIGN

Critical road blocks for Analog Design Automation

- Digital libraries too complicate to become stable between technology steps
- Huge investment in analog libraries not justified by limited use
- Insufficient time to document accurately each analog IP
- “Cultural” difficulty for analog designer to document his work/use poorly documented cells

With slowing down of Moor’s Law (Sweet Spot Technology) Analog Design Automation may become real

New bread of SOFTER analog designer may appear

RISKS OF TECHNOLOGY EVOLUTION
ESPECIALLY FOR ANALOG /RF DESIGN

Huge costs (especially mask cost)
reduces R&D and possibly stops access to Universities

- Slowing down Innovation
- Reduced number of well trained designer for Industry

- Slowing down of technology migration and integration (SOC)
- Slowing down introduction of new systems on the market

More General Risk

Slowing down progresses in Information society

EVOLUTION OF IC TECHNOLOGIES
FOR ANALOG /RF CIRCUIT DESIGN

Limitations for Analog/RF

- Increased Variability
- Worse Transistor Matching
- Larger 1/f Noise
- Smaller Gain per stage
- Fewer topology at low supply

Advantages for Analog/RF

- Faster Trans (Ft/Max THz)
- Smaller switching delay delays
- Larger 1/f Noise
- Super matched passives
- Very high Trans Q

New approach required

- Digitally intensive
- Digitally assisted
- Adaptively calibrated/corrected
- Closed loop operation beyond GHz

Still “Analog Thinking” is Mandatory for Success

Thomas Ernst

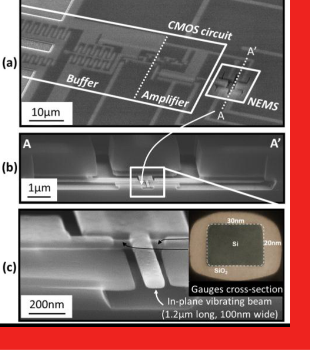
CEA-LETI

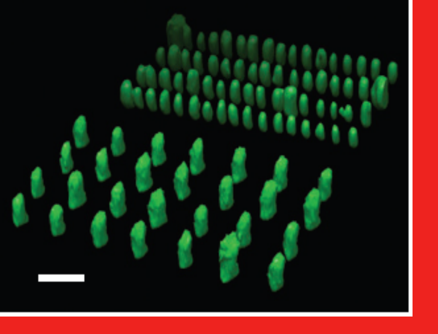
FROM RESEARCH TO INDUSTRY

FROM INTEGRATED CIRCUITS TO INTEGRATED SYSTEMS

THOMAS ERNST

Montreux
Symposium on emerging trends in electronics
1/12/2014





IC technology research – is this the end ?
No : several new market drivers

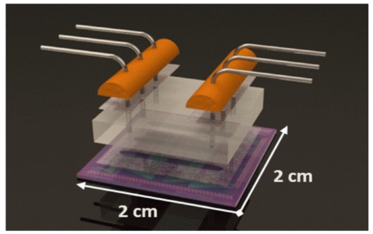
- Autonomous or ultra low power SoC-SiP (IoT, …) and related servers

LETI, 2014 IEEE WF on IoT

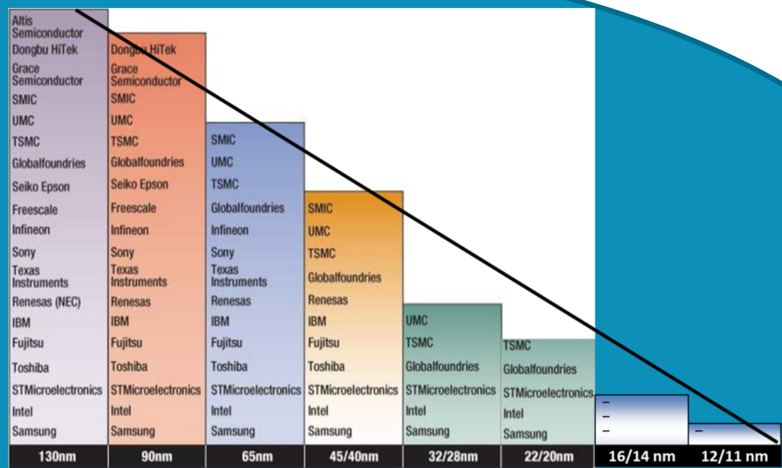
- Automotive

Google

- Health & Biochips



EPFL / LETI collab.
2014 IEEE Nano



Major semiconductor suppliers' **advanced CMOS logic manufacturing** technology capability in 2011. *(Source: IHS iSuppli)*

IC research technology drivers

5-10 years

Device Centric Evolution (scaling)

- CMOS Scaling
- NVM & embedded memory
- RF/analog/high voltage …

15 years …

System centric Heterogeneous systems

- Advanced 3D
- New materials for advanced options
- Low power (FDSOI, steep slope…)
- Emb. RRAM, MRAM, NEMS RF & Switches
- Energy sources and management
- Embedded optics
- Embedded sensors (bio, etc.)
- Safe electronics (automotive, air, space)

25 years …

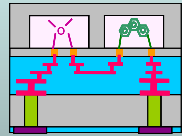
Breakthrough in data treatments

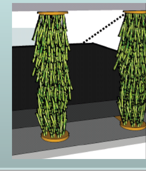
- Inexact computing
- Neuromorphic
- Quantum computing ?
- SET, Mott , Spin, …
- Bio computing?
- Adiabatic ? ..others

3DIC evolution, for low consumption, high performances

5- 15 years
Advanced concepts

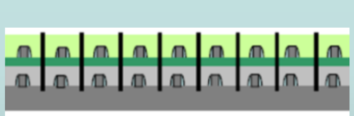
- Novel computing paradigms
- Beyond CMOS hybridization
- Bio-inspired 3D process



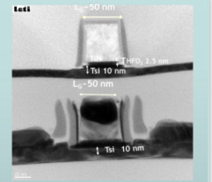


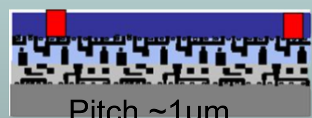
0 -10 years
The alternative to “More Moore” scaling

- Logic-on-Logic :
  (Monolithic and 3D-Stacked)
- Monolithic 3D memories
- PHOTONICS
- RF/MEMS – ANALOG
- Biochips
- Novel substrates

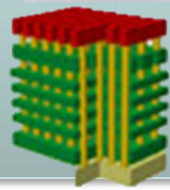


Pitch <0,1µm



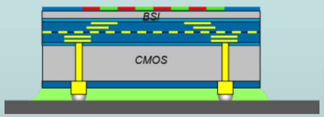


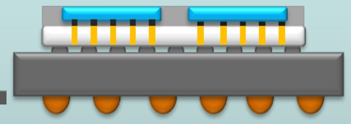
Pitch ~1µm

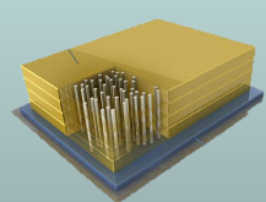


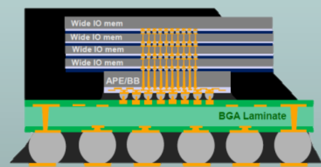
Today
The packaging evolution
Heterogeneous Era

- Si/Smart Interposers
- Memory on Logic
- Logic on analog
- MEMS on logic
- RF/ANALOG
- 3D imagers
- Biochips





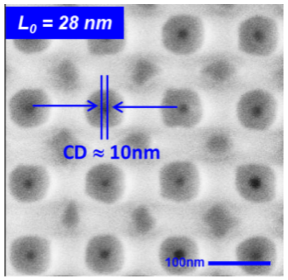


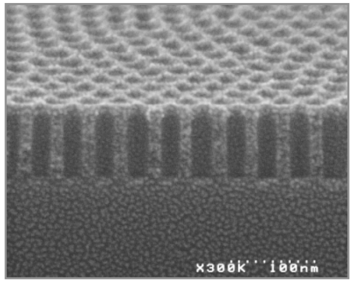


Some breakthroughs:toward integrated systems

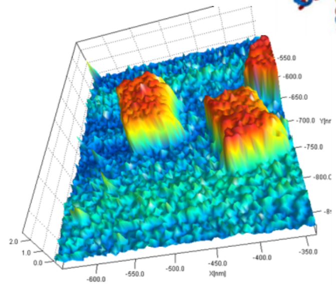
- How to connect /pattern heterogeneous devices at low cost with several types of interconnections

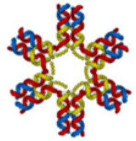
Polymers nano-contacts



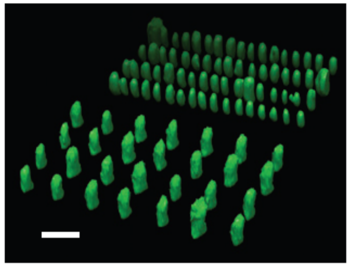


DNA

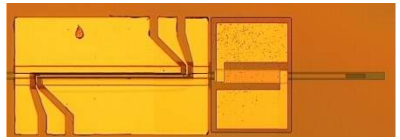




Proteins contacts

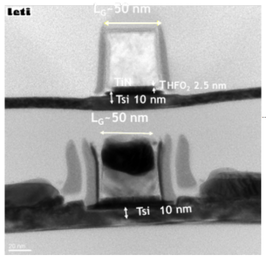


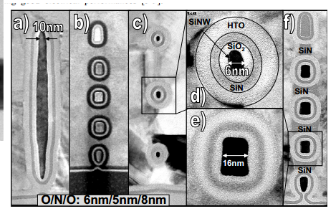
Photonics

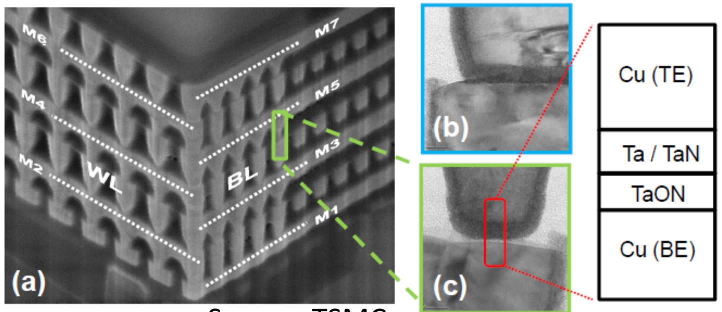


(III-V on Si)

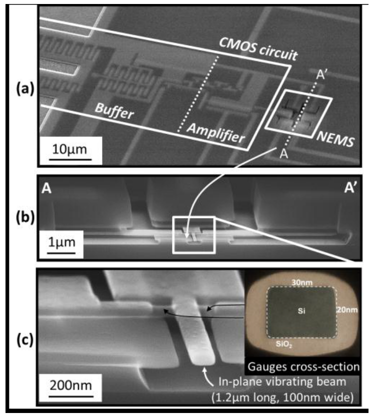
- FUSION : Embed Logic + memory + nano-systems







Source: TSMC



Ultra-dense 3D

3D Memory in a via

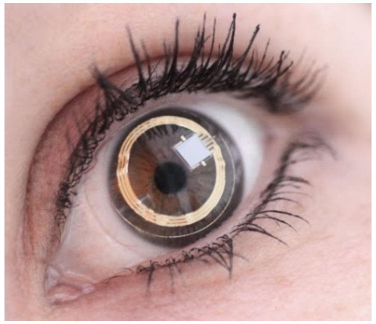
Sensors in CMOS

Source: LETI

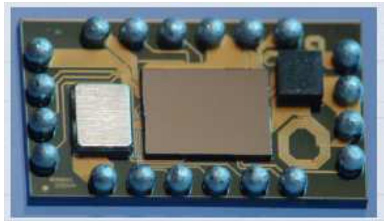
E-Health

Collaborations: Philips, Infineon, Siemens, Sorin, STMicroelectronics, Ipdia , Biomerieux …

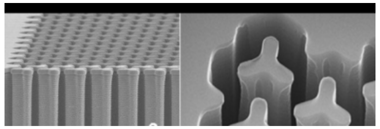
STMicroelectronics



- Flexible substrate integration
  - Interco & RDL flexibles
  - Integrated antenna on foil



- U Low power:
  - 65nm ➔ 28nm FDSOI
  - RFID , RF supply

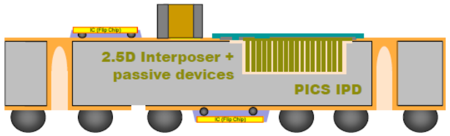


- Biocompatibility & hermetic packaging

  Intégration & passivation wafer level

- Ultra-small high performance passive
  - capa3D: 1µF/mm2

ipdia
The 3D Silicon Leader



Seok-Hee Lee

SK-Hynix

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Symposium on Emerging Trends in Electronics

Session 1 : Emerging Technologies - Circuits and Devices in the Nano Era
Panel : Circuits in Emerging Nanotechnologies

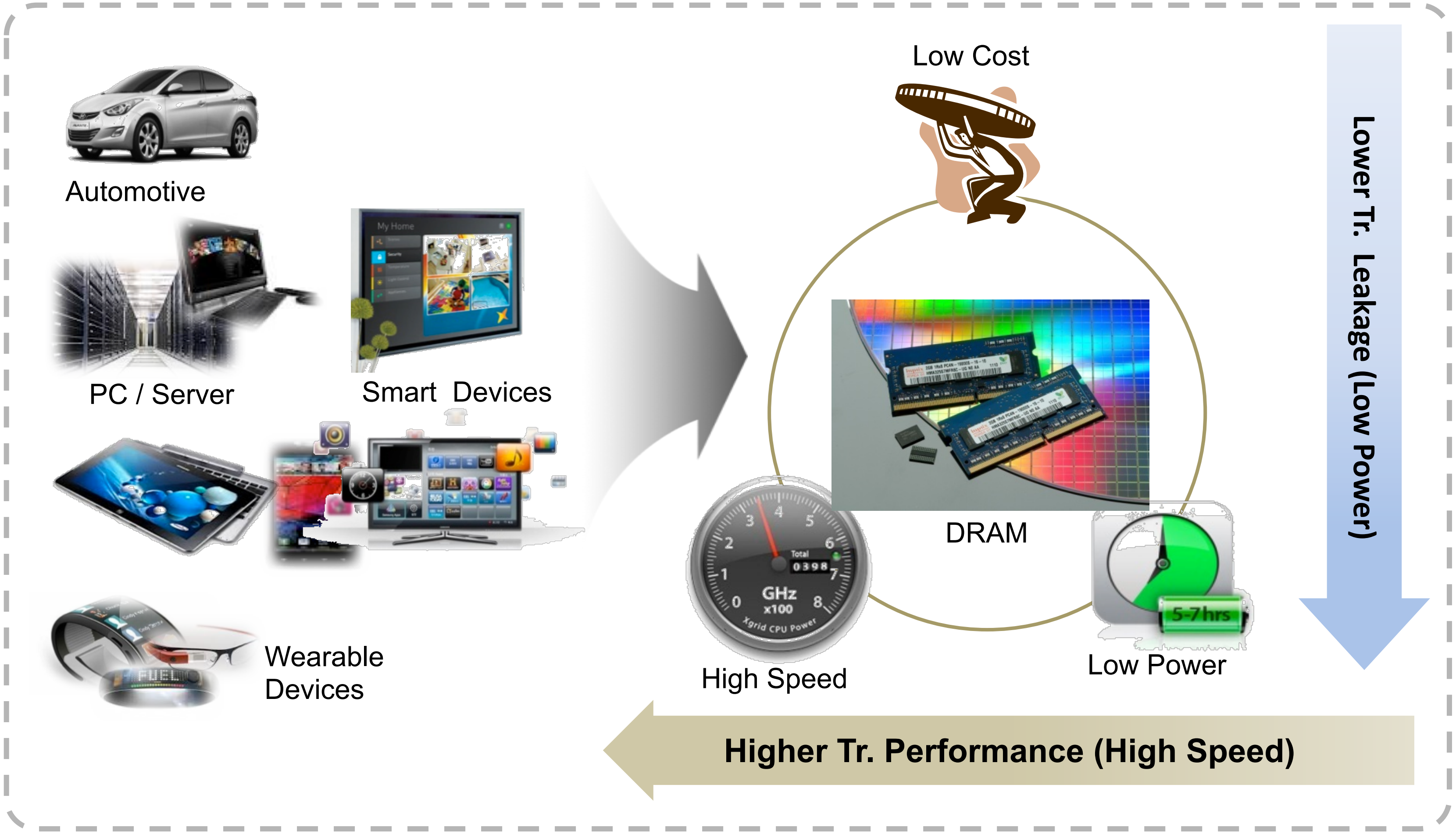
Design for
Low power & High performance DRAM

2014. 12. 1

Seok-Hee Lee
R&D Division, SK hynix

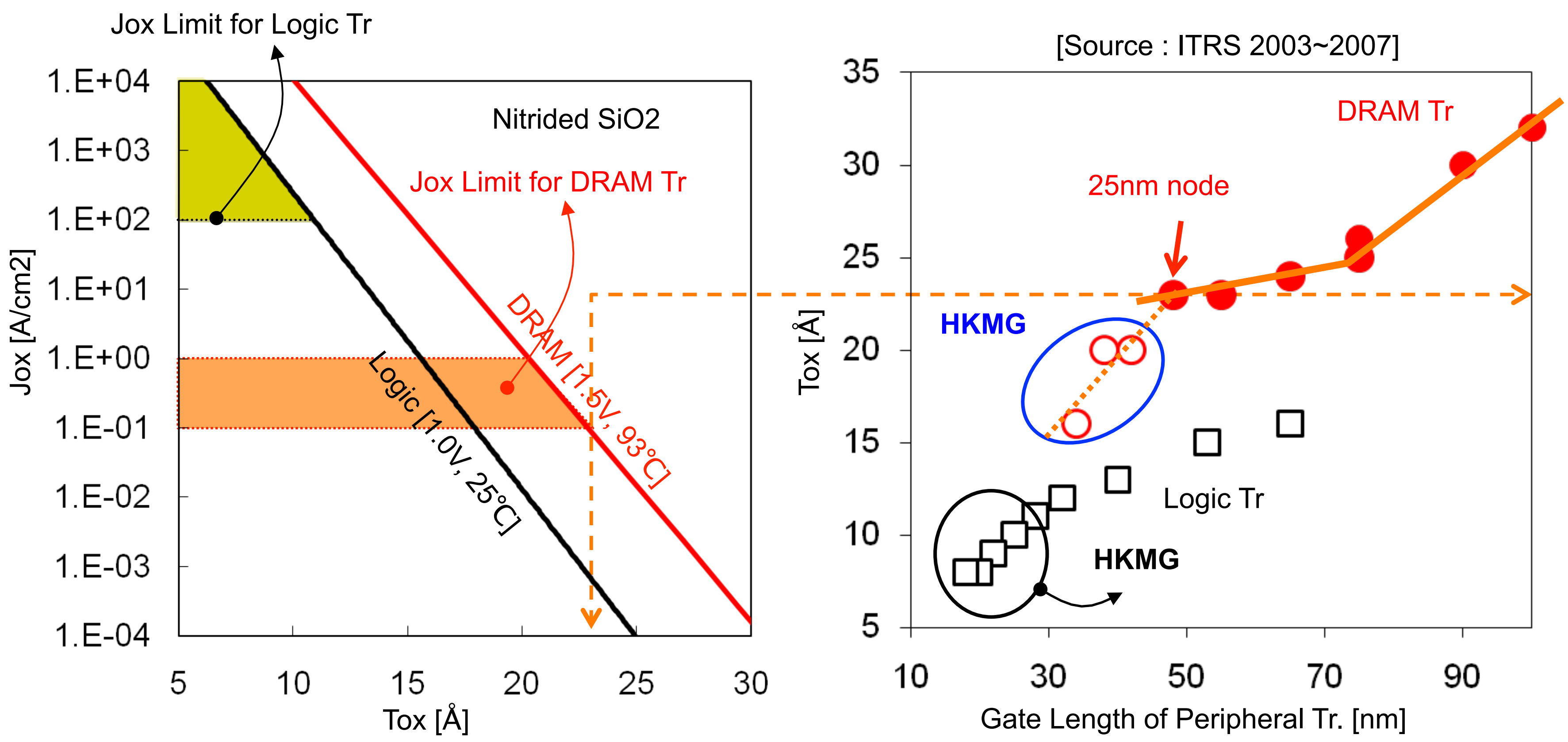
Memory demand split across multiple sub-segments

A variety of device will appear and high performance & low power DRAM will be needed as one of the most important roles in the system



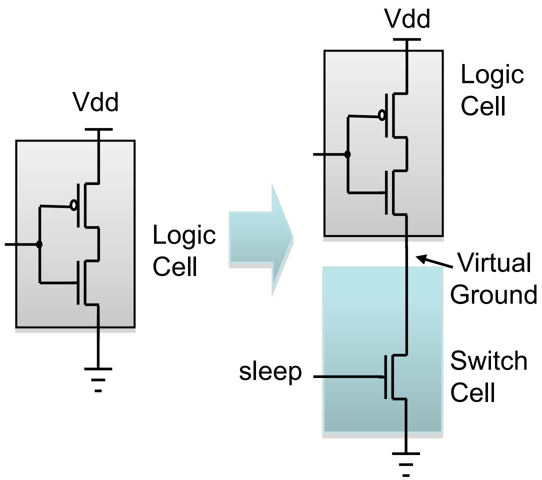
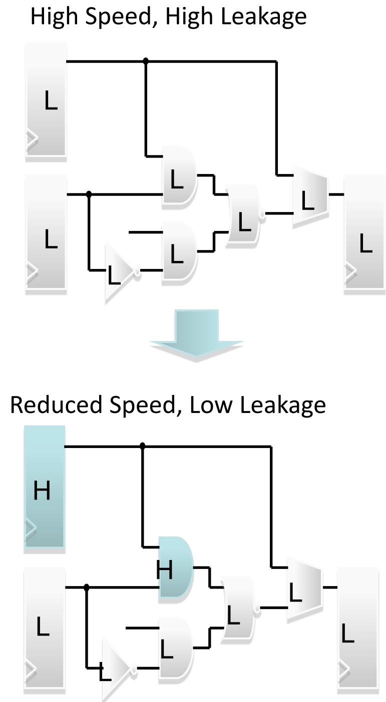
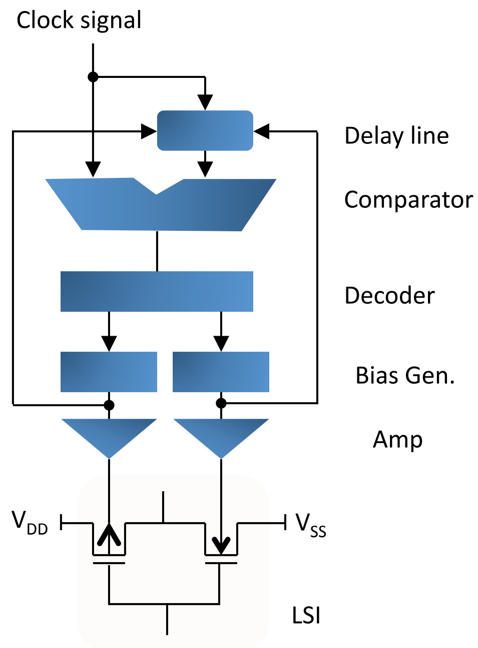
Transistor for Higher performance & Lower Power

Needs higher performance peripheral transistor for DRAM and it is affected by the slow scale-down trend of Tox



Low Power DRAM design Technique example

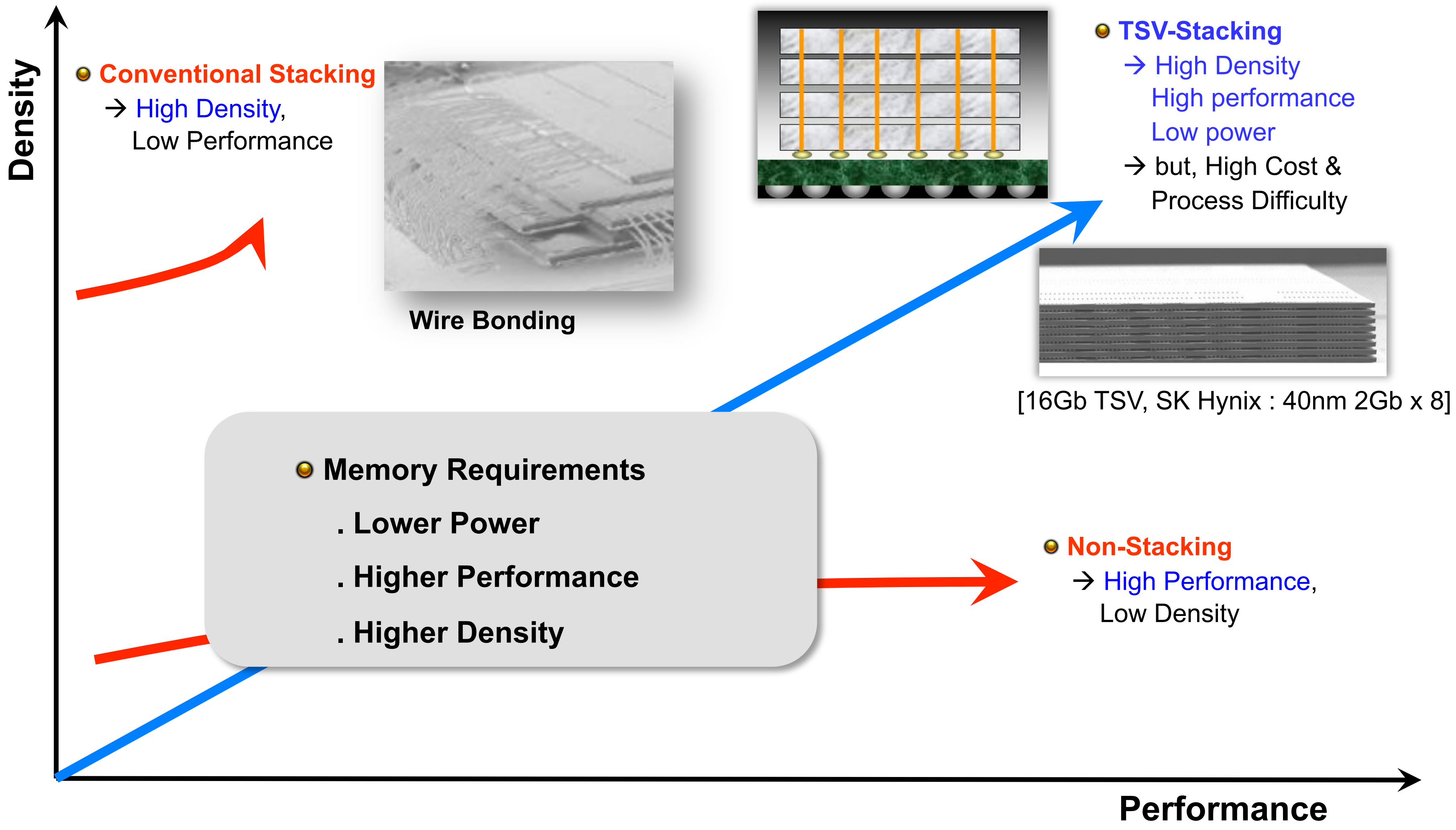
Various circuit technique is being studied for low power DRAM

	Power Gating	Multi-VTH	Dynamic Body Bias
Objective	Reduce leakage currents by inserting a switch transistor into the logic stack	Reduce leakage power where speed is not needed by high Vt transistor	Controlling body bias, high speed & lo w leakage current can be achieved
Scheme			

[Source : Low Power Design Methodology and Design Flow- JAN M. RABAEY & M. Miyazaki e al, A 1.2GIPS/W uProc using speed-adaptive Vt CMOS]

Solutions for Higher Performance & Higher Density

Require higher speed, less I/Os scheme due to process difficulty and high cost of TSV



High Reliability & Low Cost DRAM

Require cost reduction through decreasing defect rate by On-Chip ECC, PPR, etc.

	Item	Objective	Effect, Status	Issues
DFR (Design For cell Reliability)	Advanced Refresh	Refresh	Compensate Retention Time Degradation	Increase IDD
	Smart Refresh	Refresh	Improve LtRAS	
	VBB Temp Modulation	Write	Write Recovery Time	
	POD (Post Over Drive)	Refresh	Compensate Sensing Margin	Increase IDD
	On chip ECC	Error	Correction	Area Overhead
	PPR (using ARE)	Error	Aging Fail	

Subhasish Mitra

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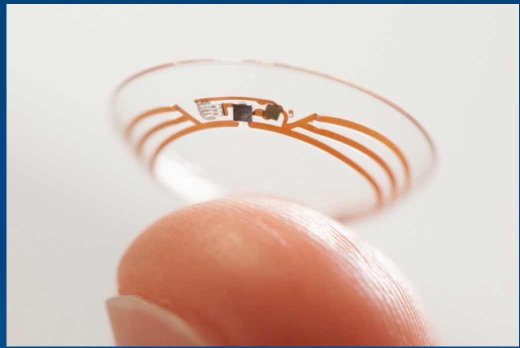
The Next *1,000X*

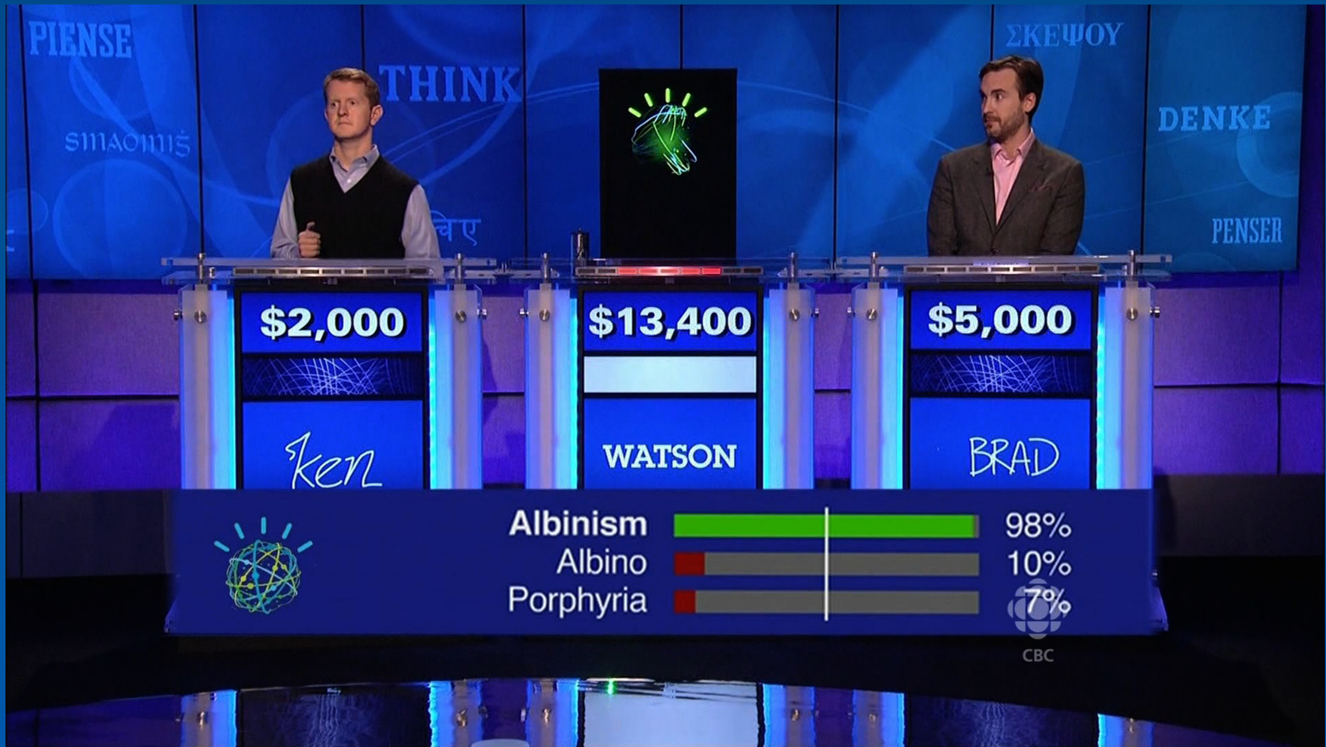
Subhasish Mitra

Collaborator: H.-S. Philip Wong

Department of EE & Department of CS
Stanford University

Abundant-Data Applications





N3XT *1,000X* Energy Efficiency

3D Resistive RAM

Massive storage

Carbon nanotube FET

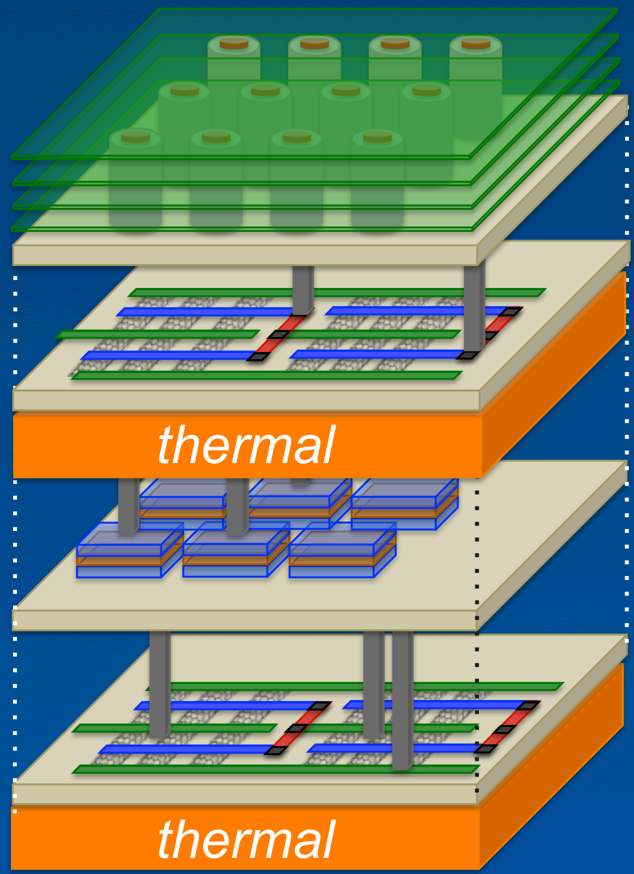
compute elements

STTRAM

L2, L3, …

Carbon nanotube FET
(or even silicon)

compute elements



Monolithic 3D

Inter-layer vias:

1,000X TSV density

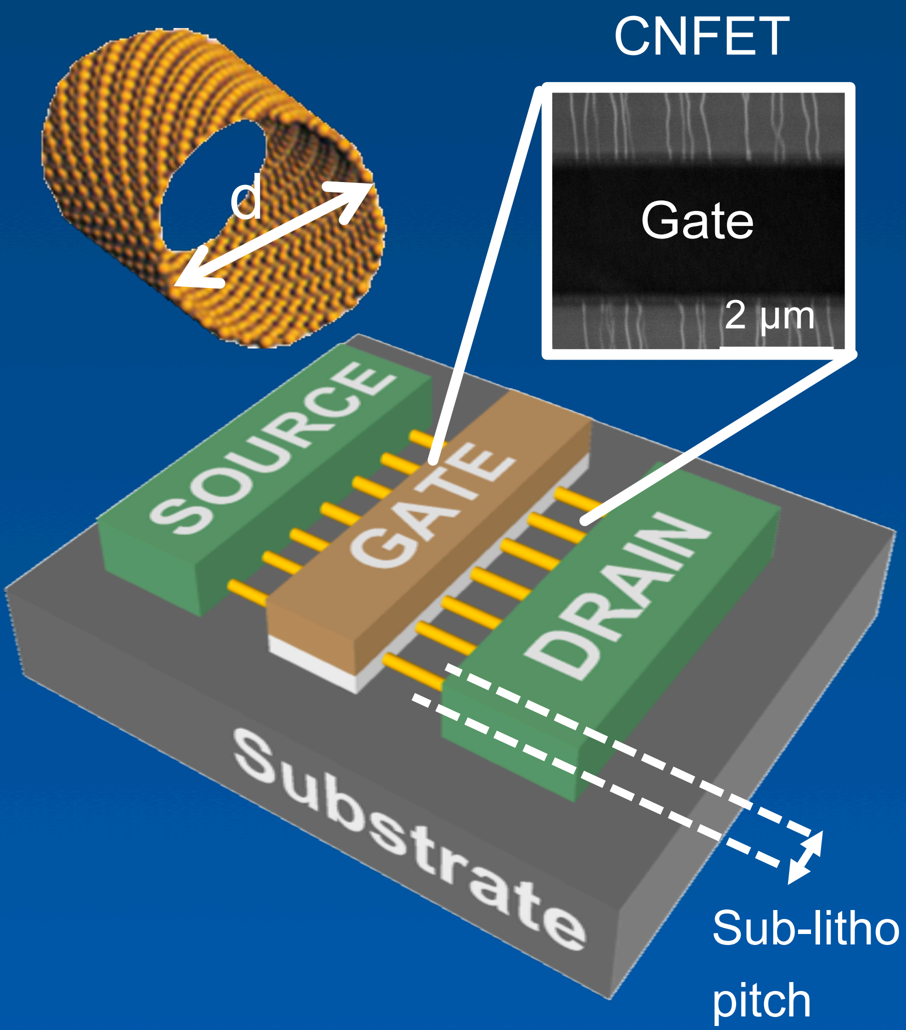
1. All data *active* on-chip

2. Computation immersed in memory

3. Variability, yield, reliability

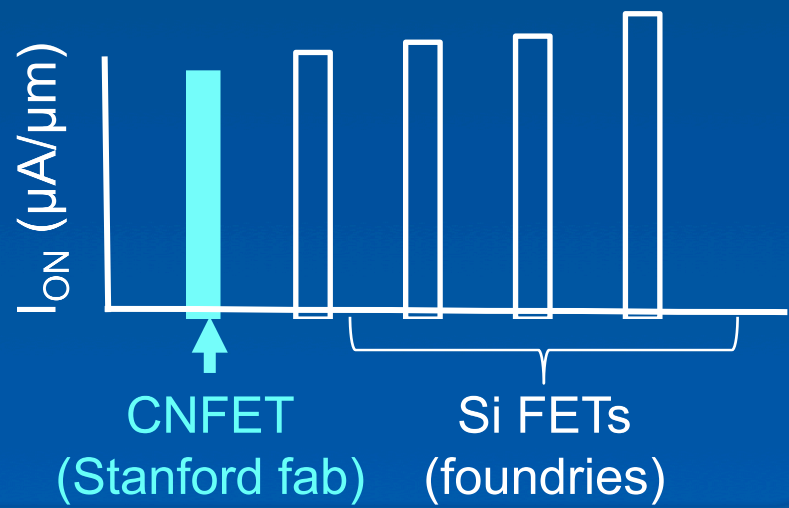
Carbon Nanotube FET (CNFET)

CNT: d = 1.2nm



1. First CNFET computer

2. High-performance CNFETs

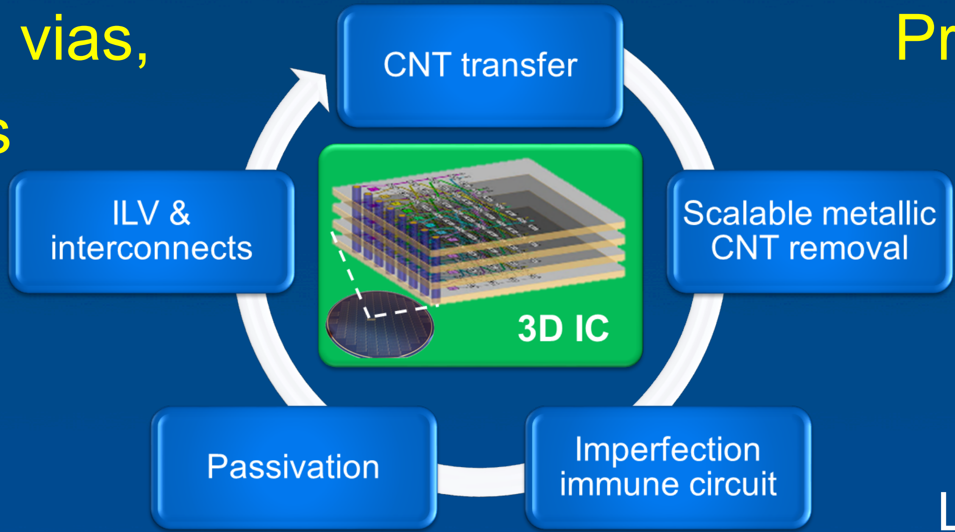


[Shulaker Nature 13, ISSCC 13, IEDM 14]

First CNT Monolithic 3D IC

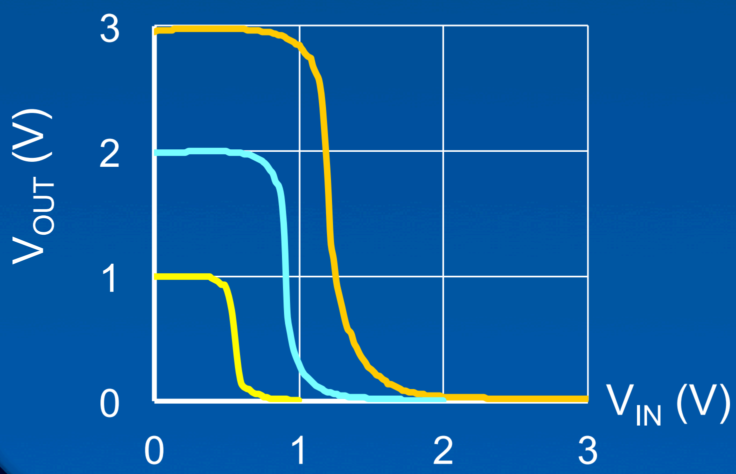
Conventional vias, no TSVs

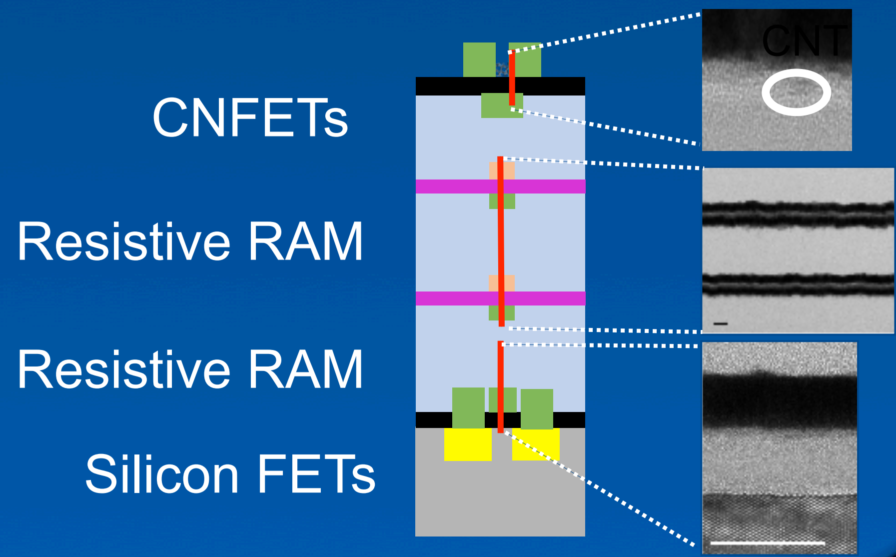
Process temp. < 250 °C



Logic + memory

Inter-layer digital circuits





[Wei IEDM 13, Shulaker VLSI Tech. 14, IEDM 14]

Ian O'Connor

Ecole Centrale de Lyon

Five Grand Challenges for Circuits in Emerging Nanotechnologies

Prof. Ian O'Connor
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Institut des Nanotechnologies de Lyon
Université de Lyon – Ecole Centrale de Lyon

Five grand challenges

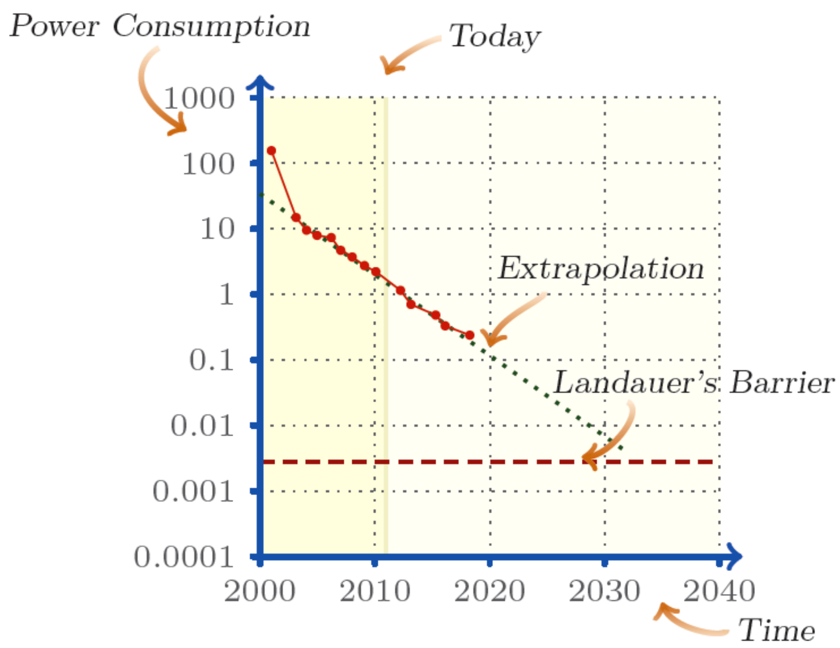
1. Reduce energy consumption and increase energy efficiency of data processing
2. Use technology to its limit throughout its life cycle, and ensure reliable system operation in the presence of both unreliable devices and increasing complexity
3. Develop hardware solutions for ZB data storage suited to the big data era
4. Develop systems adapted to new services (M2M, IoT, cloud computing ...)
5. Promote and exploit the potential of 3D heterogeneous integration

Energy

- @22nm
  - switching 1 bit in a transistor costs:

    ~1-10 aJ
  - Moving a 1-bit data on silicon costs:

    ~1 pJ/mm
- >GHz switching
- >G transistors/cm^2
- 10^3 above theoretical limit (Von Neumann-Landauer bound)



Source : R. Drechsler, U. Bremen

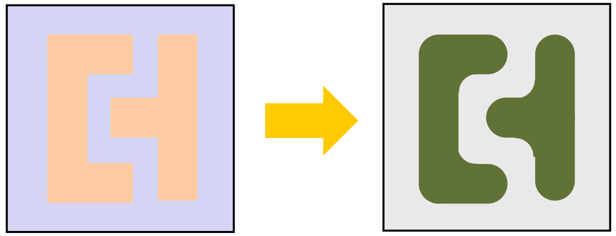
k.T.ln(2)

≈**3 zJ (3×10^{-21}J)**

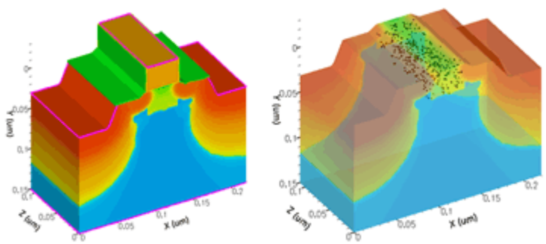
@300K

Reliability

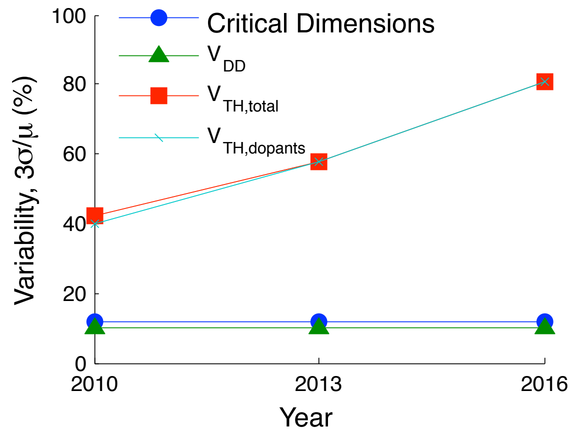
- Systematic variability (e.g. proximity effects) can be compensated physically
- Random variability cannot be compensated physically
  - Worsens with scaling
  - Compensation must be built into design
- Huge challenge
  - **3σ/μ values for threshold voltage up to 80%@22nm!**



Ex : lithography, mask correction



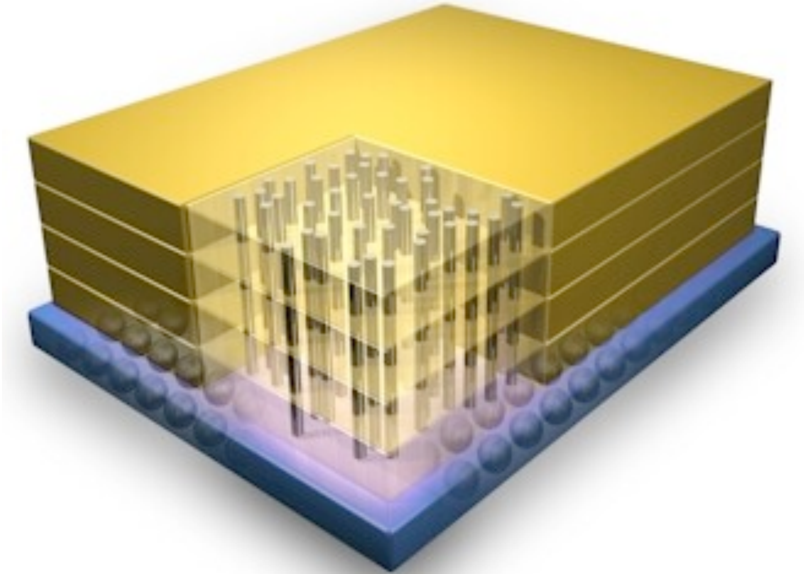
Ex : dopant concentration



Memory

- Cache hierarchies overcome distant data access issues, but at the cost of high real estate and complex management
- 3D integration of **dense, fast, low-cost, non-volatile memory** tiers (RRAM, MRAM …) could make them irrelevant

distributed memory
tiers above cores
RRAM / MRAM / SEM …



processing tier:
manycore or reconfigurable
matrix

- Configuration memory also benefits

Distributed data processing (M2M, IoT …)

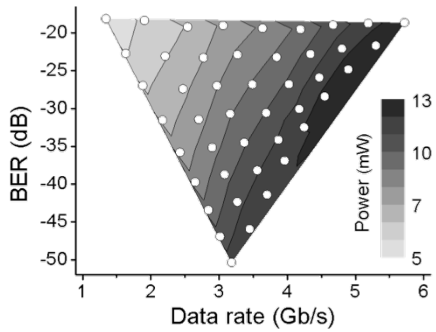
- **Ultra-low energy embedded systems**
  - Energy-constrained
  - Sense and interact with the physical environment
  - Real-time constraints
  - No intervention (intelligent, adaptive)
  - Hundreds of Mbps per mobile terminal
- **High-performance datacenters**
  - Power-constrained
  - Handling and storage of resulting exabytes of data
  - Security and reliability constraints
  - Hundreds of Gbps per node

3DICs = heterogeneity + complexity

- **Virtually infinite design space**
  - Billions of increasingly diverse and complex elementary devices
  - Nonlinear behavior of transistors, technological options
  - Multi-physics sensors/ actuators for miniaturization
  - Nanoscale devices for equivalent scaling

- Design approaches still in the Age of Great Explorers

- **Design space models bring GPS to design!**



Circuits in Emerging Nanotechnologies

Rinaldo Castello	University of Pavia
Thomas Ernst	CEA-LETI
Seok-Hee Lee	SK-Hynix
Subhasish Mitra	Stanford University
Ion O'Connor	Ecole Centrale de Lyon

Chair: Adrian Ionescu, EPFL

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Question 1

- In **which type of circuit applications (logic, memory, analog, RF, sensors with readout ICs) do you foresee an imminent role of emerging nanotechnologies** as alternative and/or complement to CMOS?
- **At which time horizon?**

  Please argue your answer.

Question 2

Today, one new technology driver, on top of the traditional scaling, is the so called **energy efficiency**.

- The question is **how much (better) energy efficiency one can achieve by emerging nanotechnologies** (for instance, using technologies allowing scaling down the voltage supply below 0.5V in logic circuits) and **how much by novel optimized design from circuit to system level**?
- How important is this topic for the future, in your opinion and **how should be addressed**?

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